TENTATIVE TOSHIBA CCD ANALOG PROCESSOR INTEGRATED CIRCUIT SILICON MONOLITHIC

TL8857F

NTSC SKEW CORRECTION IC FOR VCR

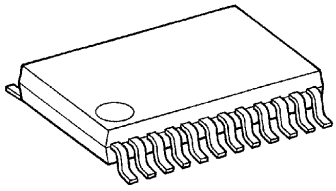
The TL8857F is the skew correction IC for the search playback signal of NTSC SP mode by 4 head PAL cylinder. This skew is made by the difference of 1H length on tape between NTSC (525 lines) and PAL (625 lines)

PAL : 625 lines = 2H

NTSC : 525 lines = (2 / 625) × 525 = 1.68H

Difference (Skew) = 2H – 1.68H = 0.32H

TL8857F corrects the skew by changing the delay time of CCD delay lines.



SOP16-P-300-1.27

Weight : 0.2g (Typ.)

FEATURES

- CCD DELAY LINES

  NTSC 0.32H / 0H DELAY LINES (Apply to both 3.58NTSC and 4.43NTSC)

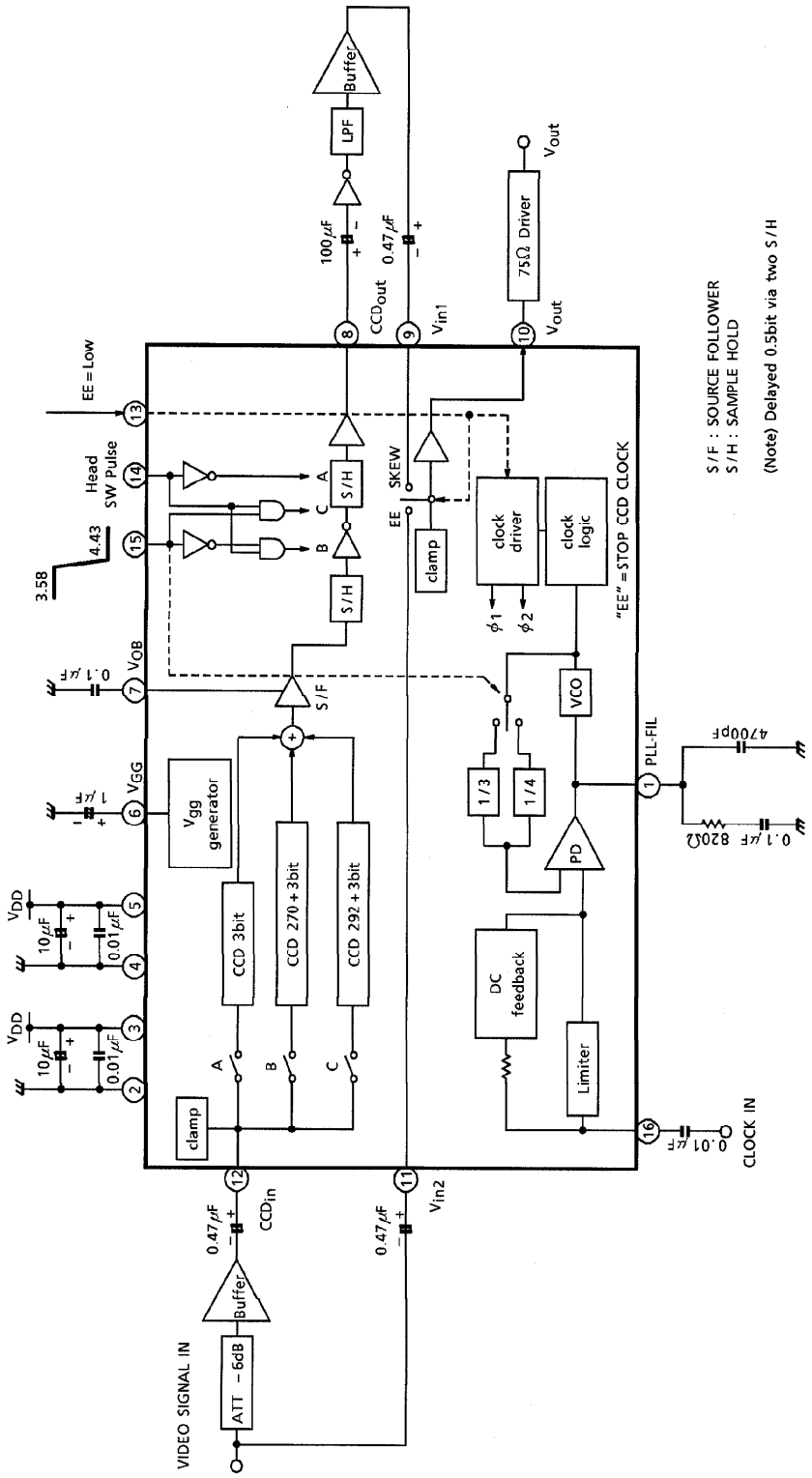
- SYNC TIP CLAMP CIRCUIT
- CCD DRIVE CIRCUIT, SAMPLE AND HOLD CIRCUIT
- 2 input SW (For the through mode)
- 2 input SW is controlled by Pin 13

  Low = Through (EE) mode
  High = Skew (correction) mode

- When Pin 13 is Low the CCD clock driver is off and the CCD output (Pin 8) is fixed to DC

- The CCD delay time is 2 mode. 0H and 0.32H, controlled by Pin 14.
  Low = 0H
  High = 0.32H
- PLL frequency multiplier is built in. 3.58NTSC and 4.43NTSC are selected by Pin 15.
  Low = 4.43NTSC
  High = 3.58NTSC
- Input signal is sampling by 4 times (3.58NTSC) or 3 times (4.43NTSC) of subcarrier frequency, generated by internal PLL multiplier.
- 5V single power supply.
- As all supporting circuit for CCD such as CCD driver, bias generators and output amplifiers are built in, minimum external parts are needed.
- The output signal at pin 8 is inverted.

BLOCK DIAGRAM



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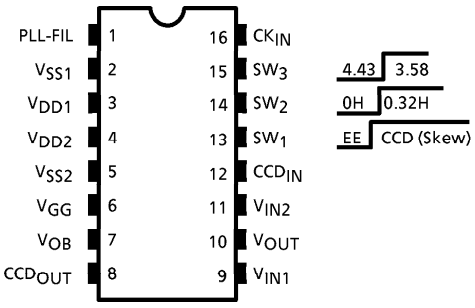
PIN LIST



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	6	V
Input Voltage	V_{IN}	$-0.3 \sim V_{DD}+0.3$	V
Power Dissipation	P_D (Note 1)	300	mW
Operating Temperature	T_{opr} (Note 2)	0~60	°C
Storage Temperature	T_{stg}	−55~150	°C

(Note 1) Ta = 60°C
(Note 2) Frost isn't to stick to the condition.

ELECTRICAL CHARACTERISTICS
DC CHARACTERISTIC (Ta = 25°C, V_{DD} = 5.0V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	V_{DD}	—		4.75	5.0	5.25	V
Supply Current	I_{DD}	—		8.0	13.0	18.0	mA
Output DC Level	CCD_{out}	—	SKEW, 3.58NTSC mode	3.0	3.6	4.2	V
	V_{OUT}		V_{in} = No signal	1.5	2.0	2.5	
Pin DC Level	CCD_{in}	—	CLOCK = 3.579545MHz	2.5	2.9	3.3	
	V_{IN1}		$300mV_{p-p}$	0.4	0.8	1.2	
	V_{IN2}		Pin 13, 14, 15 = "Hi"	0.4	0.8	1.2	
	V_{OB}		= 5V DC Input	0.9	1.5	2.1	
	PLL-FIL			0.5	1.5	2.5	
	CLOCK IN			1.3	2.3	3.3	
	V_{GG}			8.0	10.0	12.0	
Switch Input Select Level Pin Voltage	SW_{1IL}		—	—	—	1.5	
	SW_{1IH}			3.5	—	—	
	SW_{2IL}			—	—	1.5	
	SW_{2IH}			3.5	—	—	
	SW_{3IL}			—	—	1.5	
	SW_{3IH}			3.5	—	—	

ELECTRICAL CHARACTERISTICS (3.58NTSC mode, CCD part)
AC CHARACTERISTIC
(Ta = 25°C, V_{DD} = 5.0V, clock = 3.579545MHz, 0.3V_{p-p}, S_2 = 2, S_3 = 2, S_4 = 1, S_6 = 1, S_8 = 1)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
Input Level	V_{IN}	1	—			—	1.0	1.2	V_{p-p}
Voltage Gain	G_{v1}	1	S_1 = 1, S_7 = 2, S_9 = 1, S_{10} = 1, S_{11} = 2, V_{IN} = 15.625kHz, 0.6V_{p-p} (Fig.2-b)	S_5 = 2 (0H)		0	2.0	4.0	dB
	G_{v2}			S_5 = 1 (0.32H)		0	2.0	4.0	
Frequency Characteristic	G_{f1}	1	S_1 = 1, S_7 = 2, S_9 = 1, S_{10} = 1, S_{11} = 2, V_{IN} = 15.625kHz / 4.5MHz, 0.6V_{p-p} (Fig.2-b)	S_5 = 2 (0H)		– 3	– 2	—	dB
	G_{f2}			S_5 = 1 (0.32H)		– 3	– 2	—	
Differential Gain	DG1	1	S_1 = 1, S_7 = 1, S_9 = 1, S_{10} = 1, S_{11} = 3, V_{IN} = 5 step signal, 1.0V_{p-p}, Y = 140IRE = 1.0V_{p-p}, C = 40IRE (Fig.3), DG = (COmax – COmin) / COmin (Fig.5)	S_5 = 2 (0H)		—	5	7	%
	DG2			S_5 = 1 (0.32H)		—	5	7	
Differential Phase	DP1	1		S_5 = 2 (0H)		—	5	7	deg
	DP2			S_5 = 1 (0.32H)		—	5	7	
Linearity	L_{s1}	1	S_1 = 1, S_7 = 1, S_9 = 1, S_{10} = 2, S_{11} = 1, V_{IN} = 5 step signal, 1.0V_{p-p} (Fig.2-a, Fig.4)	S / Y_2	S_5 = 2 (0H)	37	40	43	%
					S_5 = 1 (0.32H)	37	40	43	
	L_{y1}	1		Y_1 / Y_2	S_5 = 2 (0H)	56	60	64	
					S_5 = 1 (0.32H)	56	60	64	
Output Impedance	Z_{01}	1	S_1 = 1, S_7 = 2, S_{10} = 1, S_{11} = 1, V_{IN} = 15.625kHz, 0.6V_{p-p} (Fig.2-b), $Z_0 = (V_1 - V_2) / V_2 \times 1000$, V_1 : S_9 = 1, V_2 : S_9 = 2		S_5 = 2 (0H)	100	250	400	Ω
					S_5 = 1 (0.32H)	100	250	400	
Clock Input Level	V_{ck}	1	—			0.2	0.3	0.7	V_{p-p}
Clock Leak (4fsc)	L_{ck} 14.3	1	S_1 = 2, S_7 = 1, S_9 = 1, S_{10} = 1, S_{11} = 2, V_{IN} = No signal		S_5 = 2 (0H)	—	20	40	mV_{rms}
					S_5 = 1 (0.32H)	—	20	40	
Clock Leak (fsc)	L_{sc} 3.58	1	S_1 = 2, S_7 = 1, S_9 = 1, S_{10} = 1, S_{11} = 2, V_{IN} = No signal		S_5 = 2 (0H)	—	1	2	mV_{rms}
					S_5 = 1 (0.32H)	—	1	2	

ELECTRICAL CHARACTERISTIC (4.43NTSC mode, CCD part)
AC CHARACTERISTIC
(Ta = 25°C, V_{DD} = 5.0V, clock = 4.43361875MHz, 0.3V_{p-p}, S_2 = 2, S_3 = 2, S_4 = 2, S_6 = 1, S_8 = 1)

CHARACTERISTIC	SYM-BOL	TEST CIR-CUIT	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
Input Level	V_{IN}	1	—			—	1.0	1.2	V_{p-p}
Voltage Gain	G_{v3}	1	S_1 = 2, S_7 = 2, S_9 = 1, S_{10} = 1, S_{11} = 2 V_{IN} = 15.625kHz, 0.6V_{p-p} (Fig.2-b)	S_5 = 2 (0H)		0	2.0	4.0	dB
	G_{v4}			S_5 = 1 (0.32H)		0	2.0	4.0	
Frequency Characteristic	G_{f3}	1	S_1 = 2, S_7 = 2, S_9 = 1, S_{10} = 1, S_{11} = 2 V_{IN} = 15.625kHz / 4.5MHz, 0.6V_{p-p} (Fig.2-b)	S_5 = 2 (0H)		– 3	– 2	—	dB
	G_{f4}			S_5 = 1 (0.32H)		– 3	– 2	—	
Differential Gain	DG3	1	S_1 = 2, S_7 = 1, S_9 = 1, S_{10} = 1, S_{11} = 3 V_{IN} = 5 step signal, 1.0V_{p-p} Y = 140IRE = 1.0V_{p-p}, C = 40IRE (Fig.3) DG = (COmax – COmin) / COmin (Fig.5)	S_5 = 2 (0H)		—	5	7	%
	DG4			S_5 = 1 (0.32H)		—	5	7	
Differential Phase	DP3	1		S_5 = 2 (0H)		—	5	7	deg
	DP4			S_5 = 1 (0.32H)		—	5	7	
Linearity	L_{s2}	1	S_1 = 2, S_7 = 1, S_9 = 1, S_{10} = 2, S_{11} = 1 V_{IN} = 5 step signal, 1.0V_{p-p} (Fig.2-a, Fig.4)	S / Y_2	S_5 = 2 (0H)	37	40	43	%
					S_5 = 1 (0.32H)	37	40	43	
	L_{y2}	1		Y_1 / Y_2	S_5 = 2 (0H)	56	60	64	
					S_5 = 1 (0.32H)	56	60	64	
Output Impedance	Z_{02}	1	S_1 = 2, S_7 = 2, S_{10} = 1, S_{11} = 1 V_{IN} = 15.625kHz, 0.6V_{p-p} (Fig.2-b) $Z_0 = (V_1 - V_2) / V_2 \times 1000$ V_1 : S_9 = 1, V_2 : S_9 = 2		S_5 = 2 (0H)	100	250	400	Ω
					S_5 = 1 (0.32H)	100	250	400	
Clock Input Level	V_{ck}	1	—			0.2	0.3	0.7	V_{p-p}
Clock Leak (3fsc)	L_{ck} 13.3	1	S_1 = 2, S_7 = 2, S_9 = 1, S_{10} = 1, S_{11} = 2 V_{IN} = No signal		S_5 = 2 (0H)	—	20	40	mV_{rms}
					S_5 = 1 (0.32H)	—	20	40	
Clock Leak (fsc)	L_{sc} 4.43	1	S_1 = 2, S_7 = 2, S_9 = 1, S_{10} = 1, S_{11} = 2 V_{IN} = No signal		S_5 = 2 (0H)	—	1	2	mV_{rms}
					S_5 = 1 (0.32H)	—	1	2	

ELECTRICAL CHARACTERISTIC Commonness (SW part)
AC CHARACTERISTIC (Ta = 25°C, V_{DD} = 5.0V, clock = 3.579545MHz or 4.43361875MHz, 0.3V_{p-p}, S_1 = 2, S_4 = 1 or 2, S_5 = 1 or 2, S_8 = 2, S_{10} = 1)

CHARACTERISTIC	SYM-BOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Input Level	V_{IN}	1	—		—	2.0	2.4	V_{p-p}
Through Mode Voltage Gain	G_{v5}	1	S_7 = 2, S_9 = 1, S_{11} = 2 V_{IN} = 15.625kHz, 1.2V_{p-p} (Fig.6-b)	S_6 = 2, S_2 = 1, S_3 = 2 (Pin 11→Pin 10)	− 1.5	− 0.5	0.5	dB
	G_{v6}			S_6 = 1, S_2 = 2, S_3 = 1 (Pin 9→Pin 10)	− 1.5	− 0.5	0.5	
Through Mode Frequency Characteristic	fth1	1	S_7 = 2, S_9 = 1, S_{11} = 2 V_{IN} = 15.625kHz / 4.5MHz, 1.2V_{p-p} (Fig.6-b)	S_6 = 2, S_2 = 1, S_3 = 2 (Pin 11→Pin 10)	− 1.0	0	1.0	dB
	fth2			S_6 = 1, S_2 = 2, S_3 = 1 (Pin 9→Pin 10)	− 1.0	0	1.0	
Differential Gain	DG5	1	S_7 = 1, S_9 = 1, S_{11} = 3 V_{IN} = 5 step signal, 2.0V_{p-p} Y = 140IRE = 1.0V_{p-p}, C = 40IRE (Fig.7) DG = (COmax − COmin) / COmin (Fig.5)	S_6 = 2, S_2 = 1, S_3 = 2 (Pin 11→Pin 10)	—	3	5	%
	DG6			S_6 = 1, S_2 = 2, S_3 = 1 (Pin 9→Pin 10)	—	3	5	
Differential Phase	DP5	1		S_6 = 2, S_2 = 1, S_3 = 2 (Pin 11→Pin 10)	—	3	5	deg
	DP6			S_6 = 1, S_2 = 2, S_3 = 1 (Pin 9→Pin 10)	—	3	5	
Linearity	L_{s3}	1	S_7 = 1, S_9 = 1, S_{11} = 1 V_{IN} = 5 step signal, 2.0V_{p-p} (Fig.6-a, Fig.4)	S / Y_2 S_6 = 2, S_2 = 1, S_3 = 2 (Pin 11→Pin 10)	37	40	43	%
				S / Y_2 S_6 = 1, S_2 = 2, S_3 = 1 (Pin 9→Pin 10)	37	40	43	
	L_{y3}	1		Y_1 / Y_2 S_6 = 2, S_2 = 1, S_3 = 2 (Pin 11→Pin 10)	56	60	64	%
				Y_1 / Y_2 S_6 = 1, S_2 = 2, S_3 = 1 (Pin 9→Pin 10)	56	60	64	
Output Impedance	Z_0	1	S_7 = 2, S_{11} = 1 V_{IN} = 15.625kHz, 1.2V_{p-p} (Fig.6-b) $Z_0 = (V_1 - V_2) / V_2 \times 1000$ V_1 : S_9 = 1, V_2 : S_9 = 2	S_6 = 2, S_2 = 1, S_3 = 2 (Pin 11→Pin 10)	100	250	400	Ω
				S_6 = 1, S_2 = 2, S_3 = 1 (Pin 9→Pin 10)	100	250	400	

TEST CIRCUIT

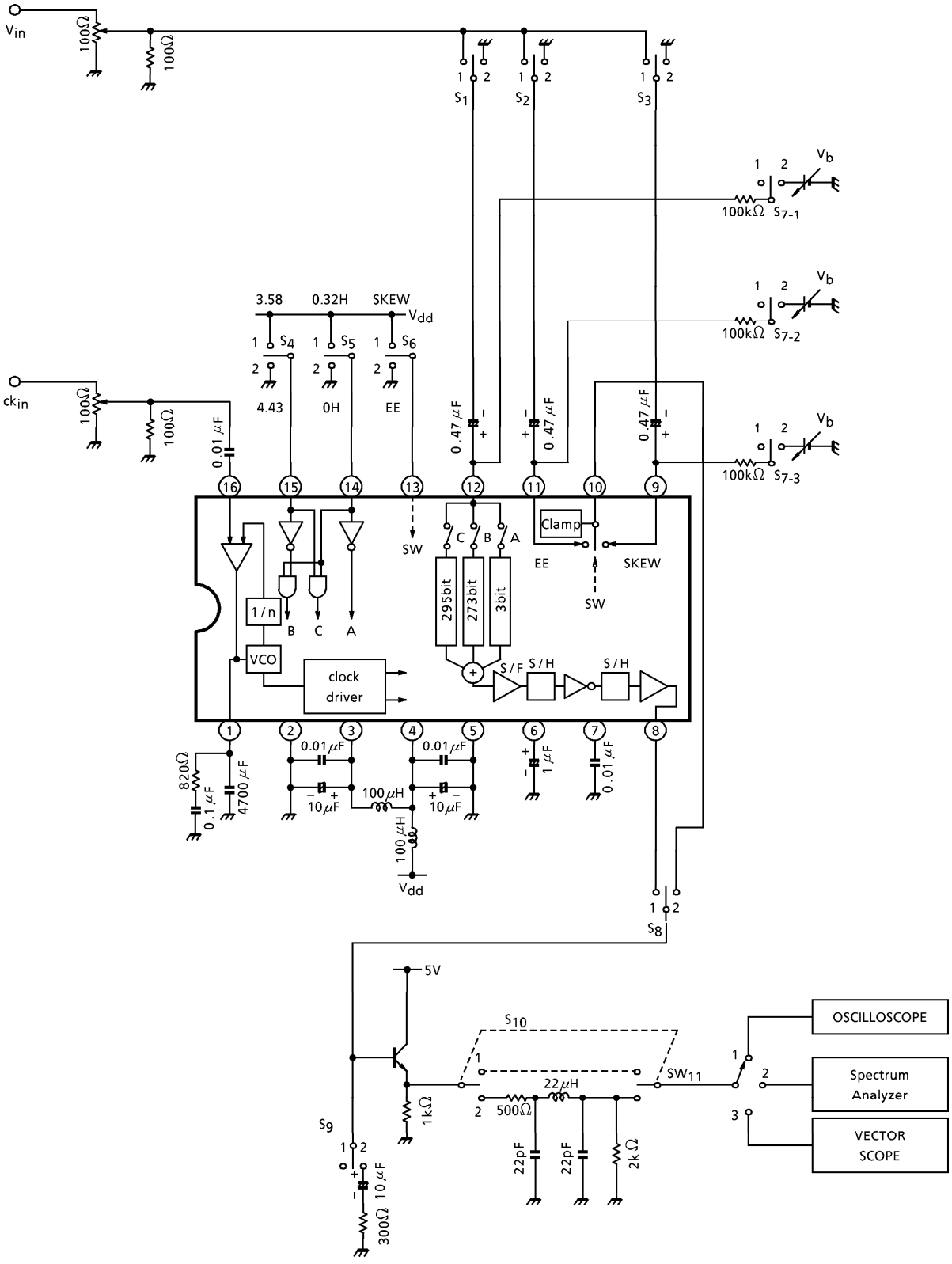


Fig.1

INPUT SIGNAL DC LEVEL

(a) 5 step staircase signal
(Clamp Operation)

(b) Sine wave input
($0.6V_{p-p}$ input)

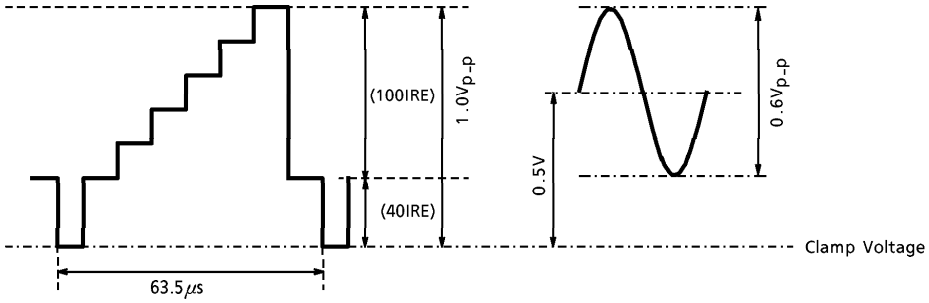


Fig.2

5 STEP STAIRCASE SIGNAL

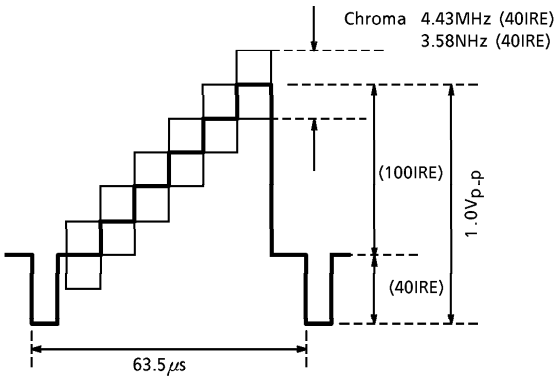


Fig.3

LINEARITY TEST SIGNAL OUTPUT

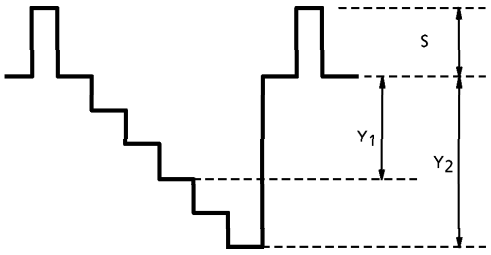


Fig.4

CHROMA DIFFERENTIAL GAIN

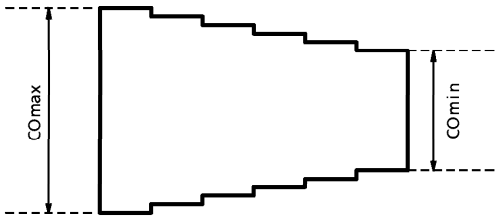


Fig.5

INPUT SIGNAL DC LEVEL

(a) 5 step staircase signal
(Clamp operation)

(b) Sine wave input
($1.2V_{p-p}$ input)

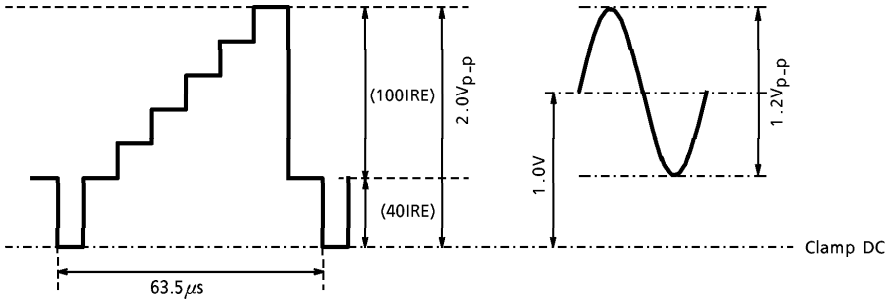


Fig.6

5 STEP STAIRCASE SIGNAL

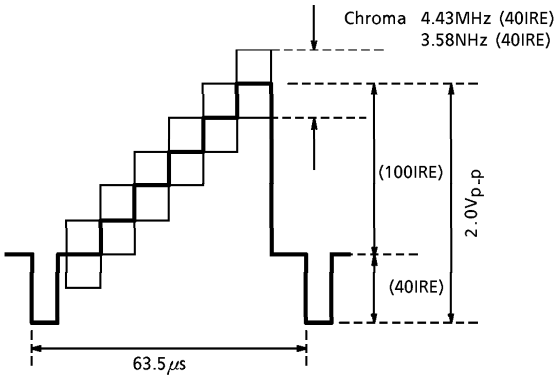
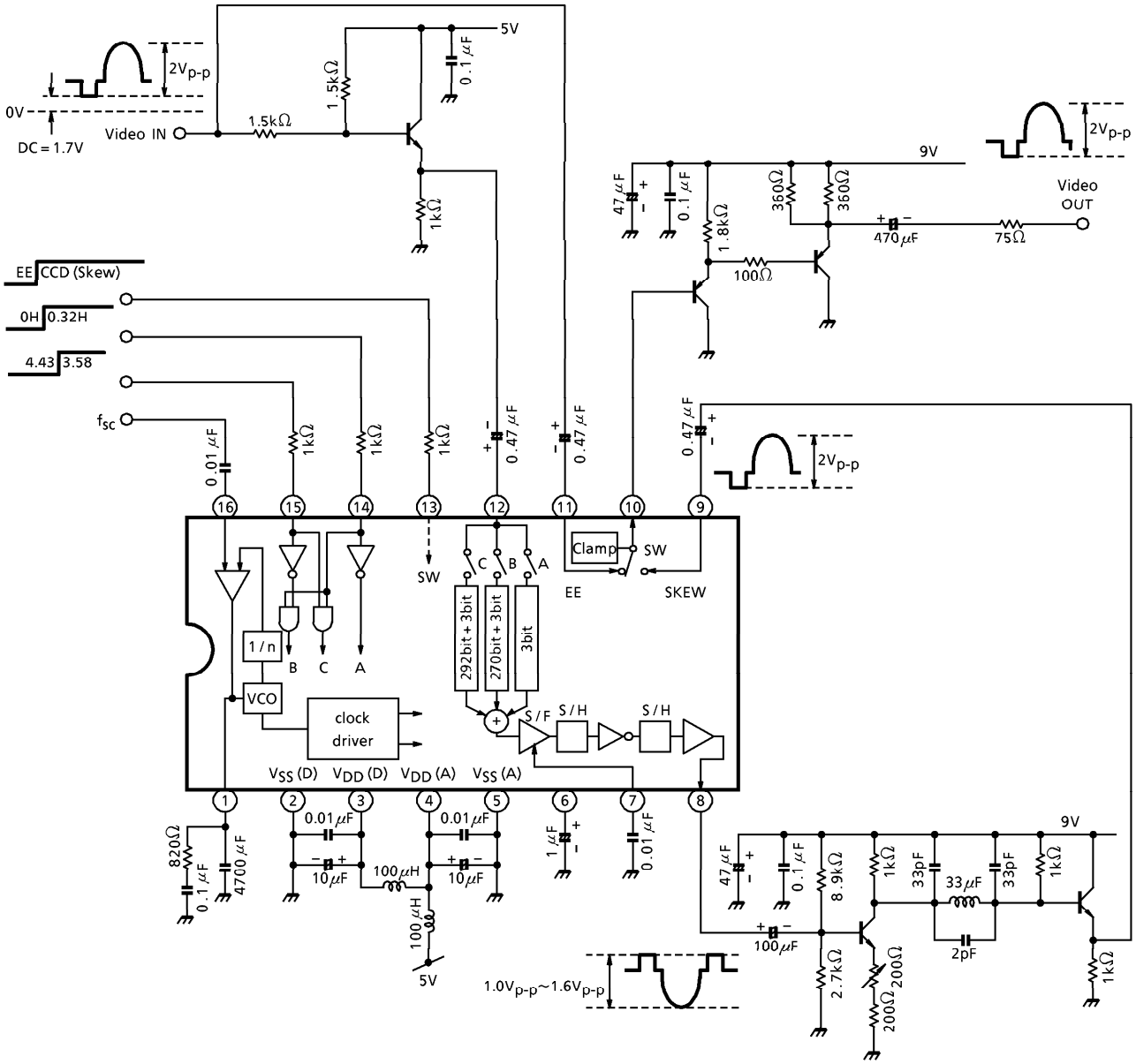


Fig.7

APPLICATION CIRCUIT



ATTENTION IN TREATMENT

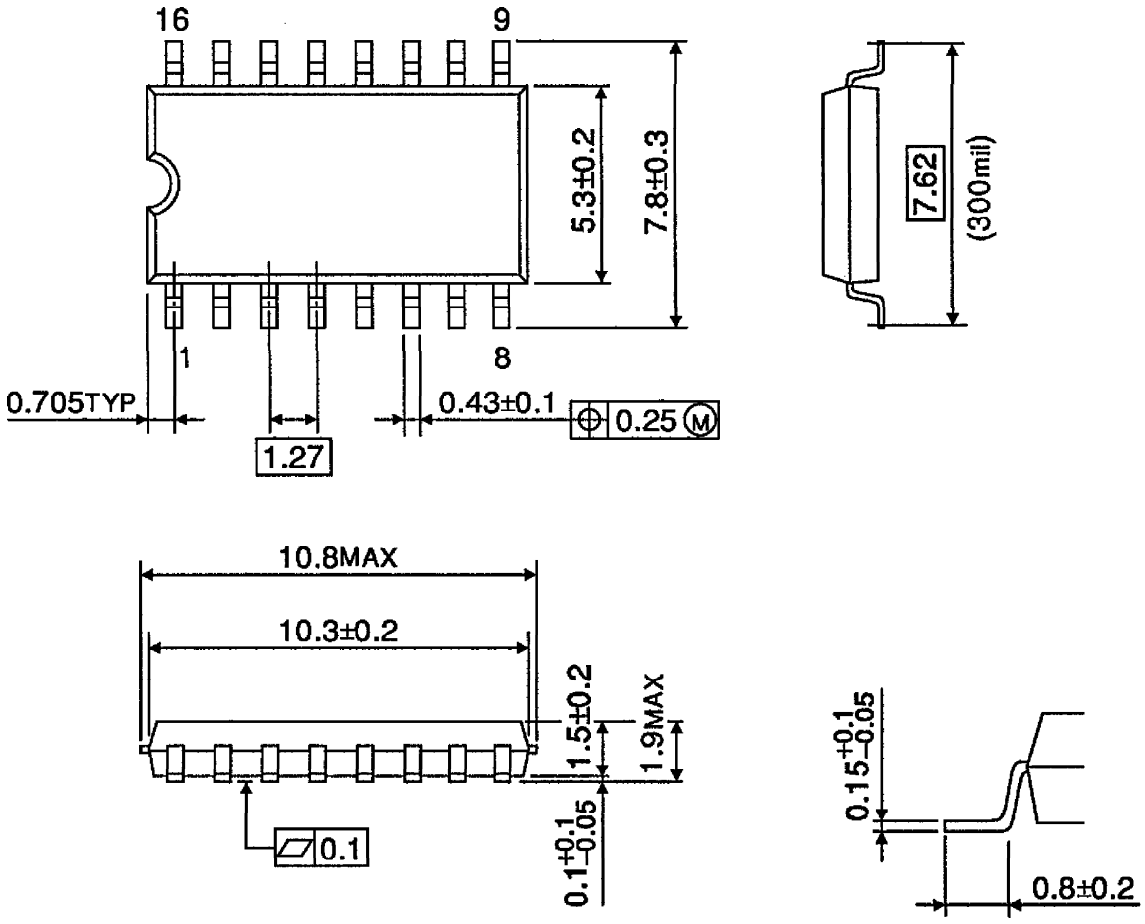
This device is electrostatic sensitive device, so care must be taken in handling and storage to prevent deterioration or damage by means of shorting electrically all pins with use of aluminum foil or conductive mat.

Even in assembled on board, it is necessary to protect against surge or inductive noise from input, output and power supply line.

OUTLINE DRAWING

SOP16-P-300-1.27

Unit : mm



Weight : 0.2g (Typ.)